
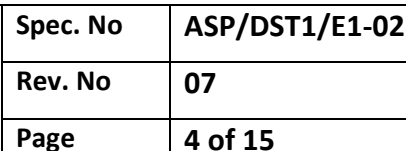
	<b>PURCHASE SPECIFICATION</b> Department: ASSCP Unit : Corporate R & D		Spec. No	ASP/DST1/E1-02	
					Rev. No	07	
					Page	1 of 15	
<b>ITEM:</b> <i>Multi Chamber Process Equipment for the deposition of amorphous silicon and Indium tin oxide layers for heterojunction solar cells</i>							
<b>COPYRIGHT AND CONFIDENTIAL</b> The information on this document is the property of Bharat Heavy Electricals Ltd. It must not be used directly or indirectly in anyway detrimental to the interest of the company			S. No.	TECHNICAL SPECIFICATION			VENDOR'S CONFIRMATION
			1.	SCOPE AND FUNCTIONAL REQUIREMENTS			
			<p>A customized system is required to deposit doped and undoped amorphous silicon (a-Si:H) and indium tin oxide (ITO) films on either 9 pseudo-square silicon wafers of size 125 mm x 125 mm or 4 pseudo-square silicon wafers of size 156 mm x156 mm in a single run, to produce a stacked structure as shown in Figure 1. The wafer thickness will be around 200 micrometer. The system will integrate plasma enhanced chemical vapor deposition (PECVD) and sputtering chambers in an in-line configuration to deposit all the layers in the sequence given in Figure 2 without breaking the vacuum. The typical thickness value for an individual a-Si:H layer will be 5 -20 nanometer and that for ITO layer will be 50 - 200 nanometer.</p> <p>The system will have one load lock, one isolation chamber, three PECVD chambers for intrinsic, p-type and n-type amorphous silicon and one chamber for ITO deposition by sputtering in the sequence as shown in Figure 2. The wafer carrier will enter the system from load lock and exit from the same load lock after the deposition of desired layers from the corresponding chambers. The transport and deposition should be computer controlled and recipe driven with the option of partial or complete manual operation.</p> <p><b>Note: The schematics are just to guide design and should not be taken as a reason for compromising the functional requirements of the system.</b></p> <p>It is intended to shut off the pumping after daily operations and start it afresh for next operation without venting in between. The base pressure and the substrate heating requirements mentioned should be attainable within 5 hours of start up.</p>				
REVISION (07)				APPROVED BY			
				S. Bhattacharya			
				CHECKED	PREPARED	DATE	
				S. P.Singh	S. Chandril		

		<div><div><div>बि एच ई एल</div><div>BHEL</div></div></div>	PURCHASE SPECIFICATION Department: ASSCP Unit : Corporate R & D		Spec. No	ASP/DST1/E1-02	
					Rev. No	07	
					Page	2 of 15	
COPYRIGHT AND CONFIDENTIAL The information on this document is the property of Bharat Heavy Electricals Ltd. It must not be used directly or indirectly in anyway detrimental to the interest of the company		S.No	TECHNICAL SPECIFICATION			VENDOR'S CONFIRMATION	
		1	SCOPE AND FUNCTIONAL REQUIREMENTS				
			The system and chamber dimensions should be optimally chosen to meet the process requirements in the respective chambers in terms of the uniformity and quality of the films. Special care should be taken in designing showerhead electrode, heating arrangement, isolation gate valves to provide a contamination-free environment in the process chambers. The vendor will provide all the items and accessories to monitor and control the system as an independent unit. BHEL scope is limited to furnishing the facility requirements such as power, water, compressed air, abatement system etc. up to a common point on the support structure of system. Process gases will also be provided by BHEL.				
		2	DETAILS OF EQUIPMENT				
		2A	Single run capability	Processing of 9 pseudo-square silicon wafers of size 125 mm x 125 mm or 4 pseudo-square silicon wafers of size 156 mm x156 mm in a single run			
		2B	System configuration	1 entrance conveyor and 6 rectangular vacuum chambers connected in In-line configuration. The vacuum chambers will be fabricated from SS 304 and will have fixtures and ports for mounting heaters, pumps, gauges, transport mechanism, power supply connections, viewing ports etc. The chambers will be electro polished from Inside and glass bead blasted from outside. Gate valves must be installed at the start of load lock, between all adjacent chambers and at the end of ITO chamber to perfectly isolate the chamber process environment from the environment of the adjacent chambers or atmosphere.			
		2C	Wafer Carrier Transport properties	a.	Speed	Variable, up to 1000 mm/min.	
				b.	Capabilities & operation	Smooth transfer of wafer carrier in both directions and full integration with the system automation.	

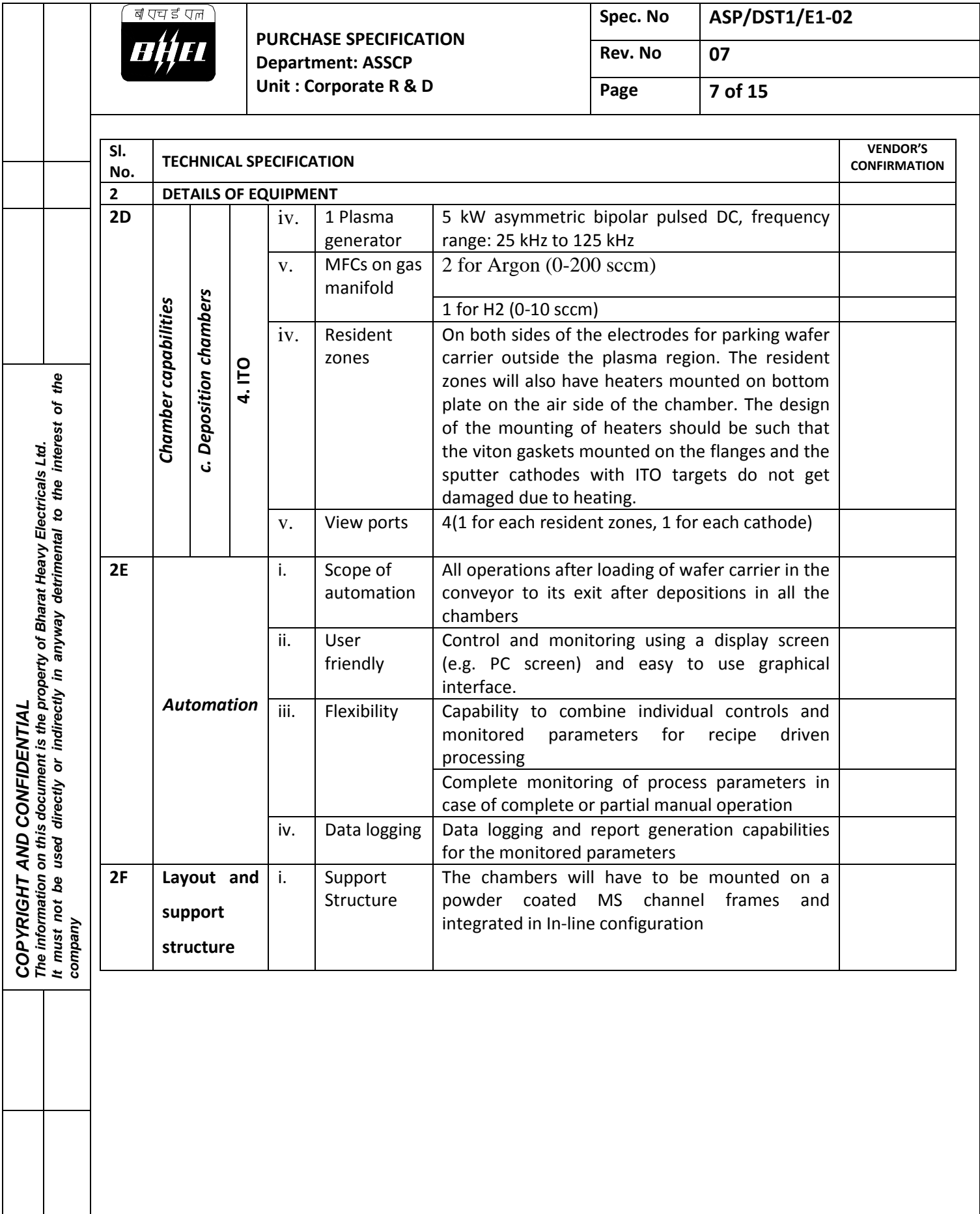
		<div><div><div>बि एच ई एल</div><div></div></div><div><div>PURCHASE SPECIFICATION</div><div>Department: ASSCP</div><div>Unit : Corporate R &amp; D</div></div></div>	Spec. No		ASP/DST1/E1-02				
			Rev. No		07				
			Page		3 of 15				
<div>COPYRIGHT AND CONFIDENTIAL</div> <div>The information on this document is the property of Bharat Heavy Electricals Ltd.</div> <div>It must not be used directly or indirectly in anyway detrimental to the interest of the company</div>		S. No.	TECHNICAL SPECIFICATION					VENDOR'S CONFIRMATION	
		2.	DETAILS OF EQUIPMENT						
		2 D	Chamber capabilities	a.	Load Lock chamber	i.	Base pressure (Torr)	< 1 x 10 <sup>-3</sup> at 150 °C substrate temperature	
						ii.	Pumping	Dry	
						iii.	Substrate Heating	~200 °C in 20 minutes using IR heaters inside the chamber or heaters mounted on the lid or bottom plate or on both on the atmospheric side of the chamber. The design of the mounting of heaters should be such that the viton gaskets mounted on the flanges do not get damaged due to heating.	
						iv.	View ports	≥ 2	
				b.	Isolation chamber	i.	Base pressure	≤ 8 x 10 <sup>-7</sup> Torr at 150 °C temperature after appropriate heating for 3-4 hours.	
						ii.	Substrate heating	350 °C in 5 minutes using Infrared heating	
						iii.	View ports	≥ 2	
						iv.	Ports with isolation valves	≥ 2, at the back side (port size : 40 KF)	
c.	Deposition chambers (Features common to intrinsic, p-type, n-type and ITO chambers)			i.	Substrate heating	Up to 325 °C during process gas flow. The wafer temperature should be controlled between 100 to 325 °C within ± 5 °C. The heaters should be mounted on the atmosphere side of the chamber. The design of the mounting arrangement of heaters should be such that the viton O-rings mounted on the flanges do not get damaged due to heating. Also chamber should not develop any cold regions in the chamber due to heater design.			



**COPYRIGHT AND CONFIDENTIAL**  
The information on this document is the property of Bharat Heavy Electricals Ltd.  
It must not be used directly or indirectly in anyway detrimental to the interest of the  
company

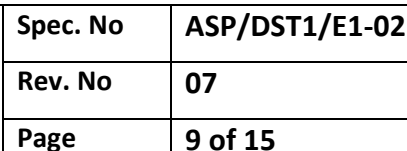


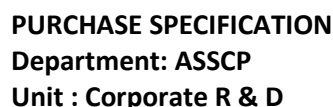
Sl. No.	TECHNICAL SPECIFICATION						VENDOR'S CONFIRMATION
2	DETAILS OF EQUIPMENT						
2D	Chamber capabilities	c. Deposition chambers	2. p-type a-Si:H	iv.	MFCs on gas manifold	1 H2, 1 SiH4, 1 TMB, 1 B2H6 with required flow rates for typical p-type a-Si:H deposition	
						1 for NF3 (0-100 sccm)	
						1 for SiH4 (0-100 sccm)	
				v.	View ports	2	
			3. n-type a-Si:H	i.	Mode of deposition	Stationary mode deposition with wafer carrier under the electrode	
				ii.	Electrode	Showerhead with dark space shield	
				iii.	Plasma source	13.56 MHz with 600 W capability	
iv.	MFCs on gas manifold	1 H2, 2 SiH4 with required flow rates for typical n-type a-Si:H deposition					
		1 for NF3 (0-100 sccm)					
		1 for SiH4 (0-100 sccm)					
v.	View ports	2					
4. ITO	i.	Mode of deposition	Moving mode deposition from top and bottom at the same time with gate valves closed on both sides of the chamber				
	ii.	2 Sputtering cathodes	1 on top & 1 on bottom; installed with a minimum horizontal separation of 200 mm				
iii.	Material	99.999% purity ITO					
		Size (mm)	length - 125 mm; width – suitable for uniform deposition on all wafers				











<b>Spec. No</b>	<b>ASP/DST1/E1-02</b>
<b>Rev. No</b>	<b>07</b>
<b>Page</b>	<b>10 of 15</b>

Sl. No.	TECHNICAL SPECIFICATION			VENDOR'S CONFIRMATION
10	Acceptance criteria	5.	Intrinsic hydrogenated amorphous silicon layers deposited by PECVD in intrinsic chamber on Corning Eagle 2000 or equivalent glass should have state of the art properties: optical band gap (Tauc) 1.65-1.75 eV, dark conductivity $\sigma_D < 10^{-10}$ (ohm cm) <sup>-1</sup> ; photoconductivity under global AM1.5 illumination $\sigma_L > 10^{-5}$ (ohm cm) <sup>-1</sup> . The film thickness should have uniformity $\pm 5\%$ over the area of 400 mm x 400 mm. The uniformity may be demonstrated on an ordinary glass.	
		6.	p <sup>+</sup> -doped hydrogenated amorphous silicon layers deposited by PECVD in P chamber on Corning Eagle2000 or equivalent glass using diborane/TMB mixtures should have dark conductivity $\sigma_D > 1 \times 10^{-5}$ (ohm cm) <sup>-1</sup> , bandgap > 1.6 eV –1.75 eV. The film thickness should have uniformity $\pm 5\%$ over the area of 400 mm x 400 mm. The uniformity may be demonstrated on an ordinary glass.	
		7.	n <sup>+</sup> -doped hydrogenated amorphous silicon layers deposited by PECVD in n chamber on Corning Eagle 2000 or equivalent glass using SiH <sub>4</sub> -PH <sub>3</sub> gas mixtures should have the dark conductivity $\sigma_D > 10^{-3}$ (ohm cm) <sup>-1</sup> . The film thickness should have uniformity $\pm 5\%$ over the area of 400 mm x 400 mm. The uniformity may be demonstrated on an ordinary glass.	
		8.	80 nm ITO layers deposited by sputtering in ITO Chamber should have the sheet resistance of 45 ohm/sq. and transmission > 88%. The film thickness should have uniformity $\pm 5\%$ over the area of 400 mm x 400 mm. The uniformity may be demonstrated on an ordinary glass.	
		9.	The transport arrangement should be smooth, snag-free and fully integrated in the automation scheme of the system. Smooth movement including transfer of the wafer carrier in the chambers.	
		10.	Automation capabilities should be demonstrated by executing the recipe driven depositions and the start up process.	
		11.	The supplier should provide list of clients and record of at least 2 successfully working custom built PECVD and sputtering equipment with the similar pressure and temperature range.	

**COPYRIGHT AND CONFIDENTIAL**

*The information on this document is the property of Bharat Heavy Electricals Ltd. It must not be used directly or indirectly in anyway detrimental to the interest of the company*

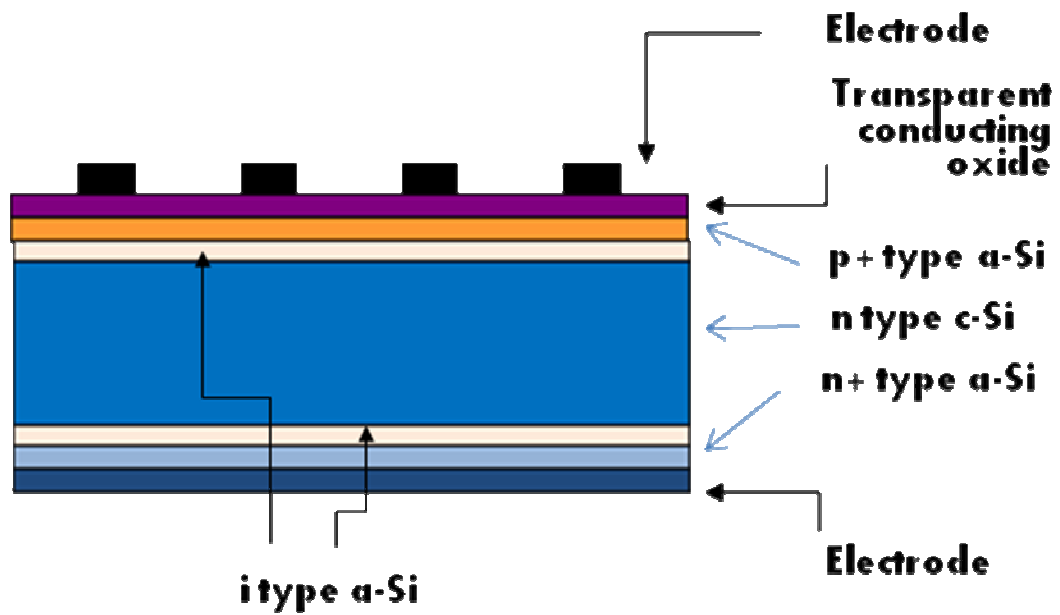
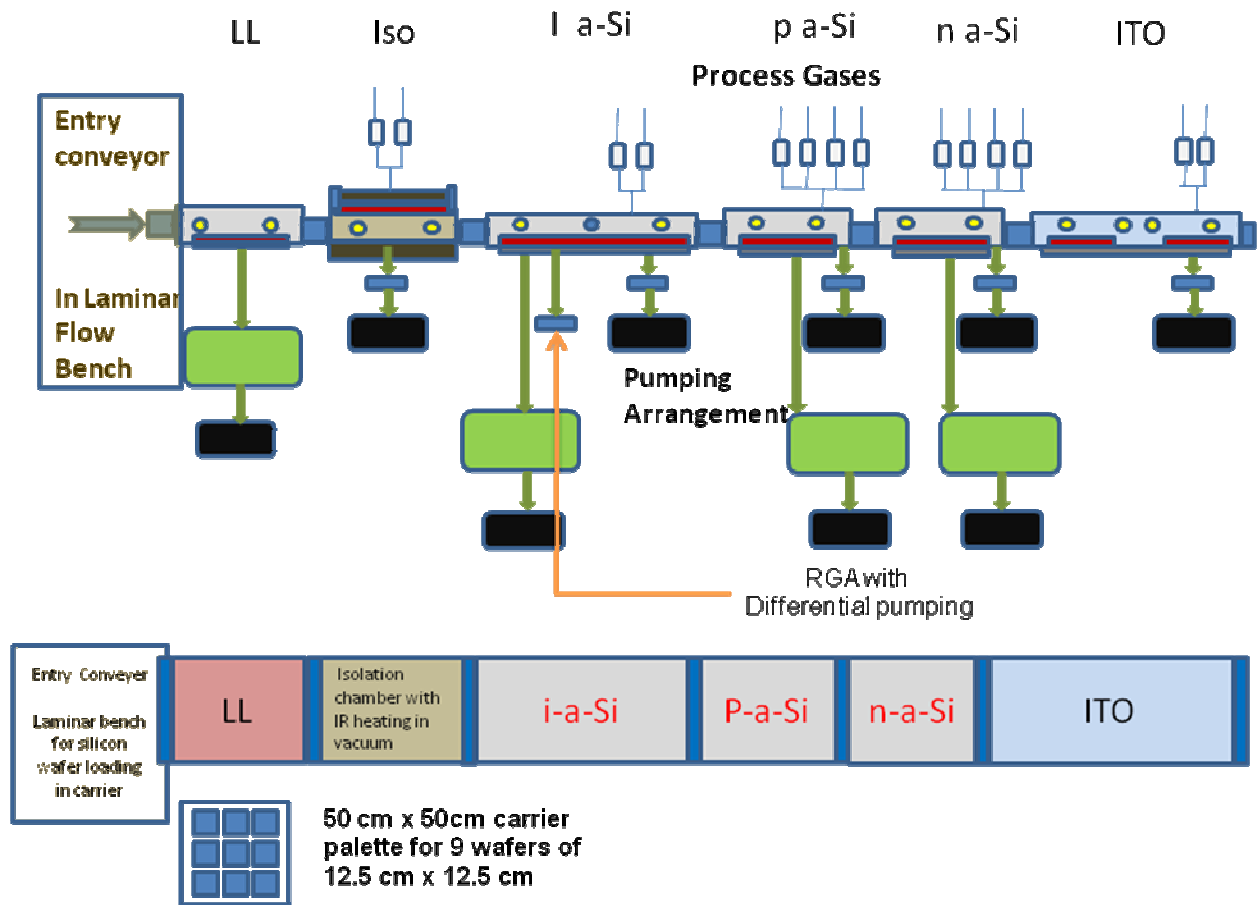


Fig. 1 Schematic of a silicon heterojunction solar cell



**Fig. 2 Schematic of the proposed In-line System**

## A-Si Process Chamber Schematics – I layer

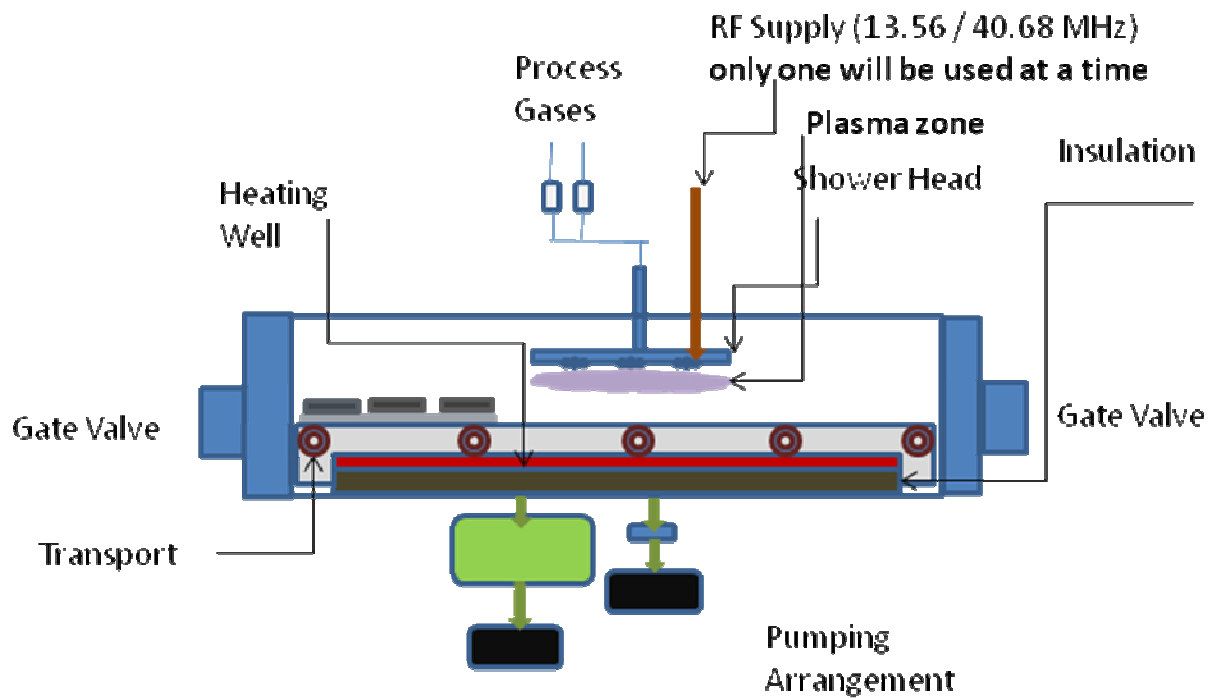


Fig. 3 Schematic of the Intrinsic a-Si Deposition Chamber

## A-Si Process Chamber Schematics - Doped layers

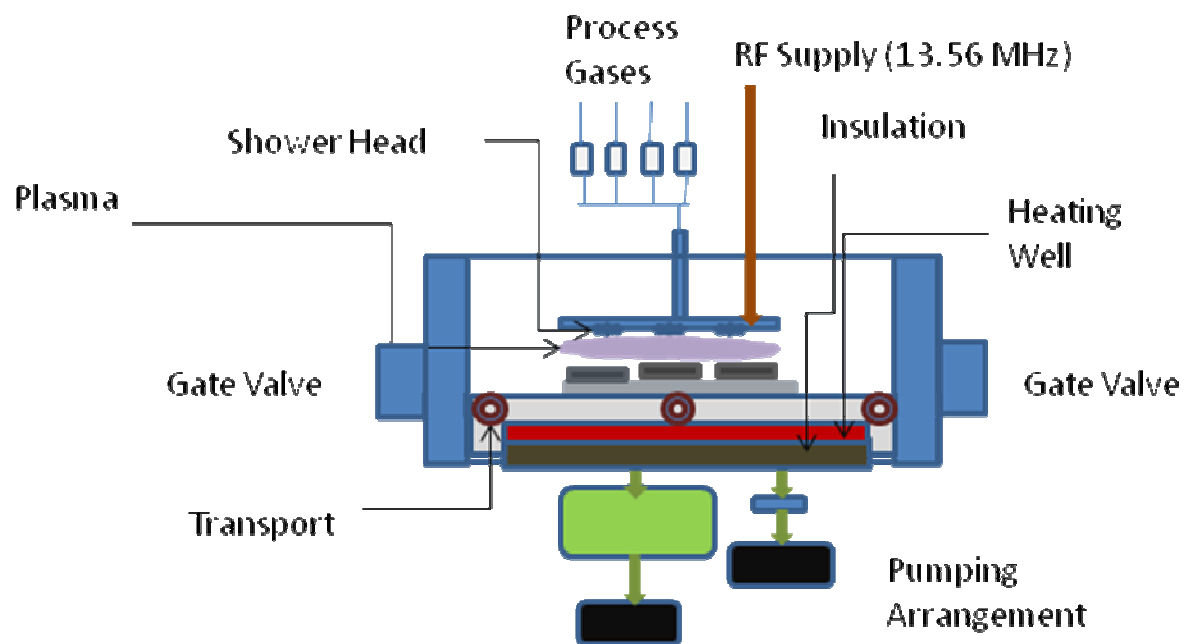


Fig. 4 Schematic of the Doped a-Si Deposition Chamber

## ITO Process Chamber Schematics

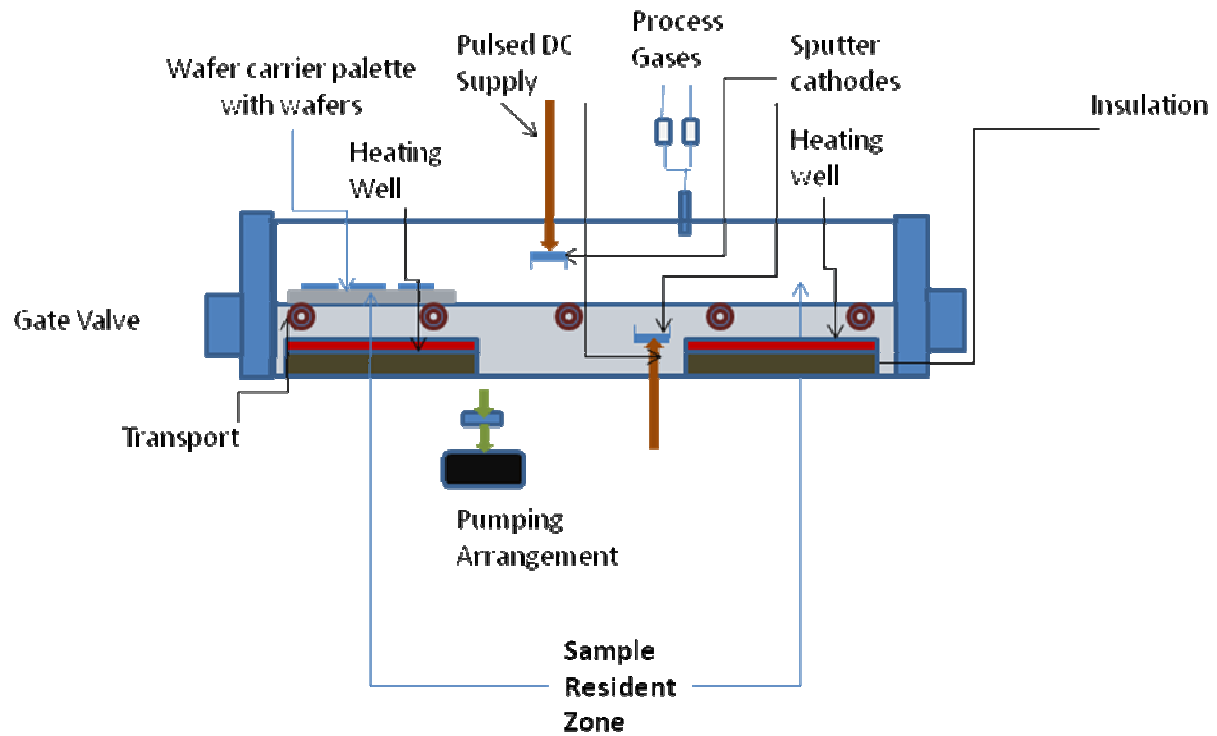


Fig. 5 Schematic of ITO Deposition Chamber